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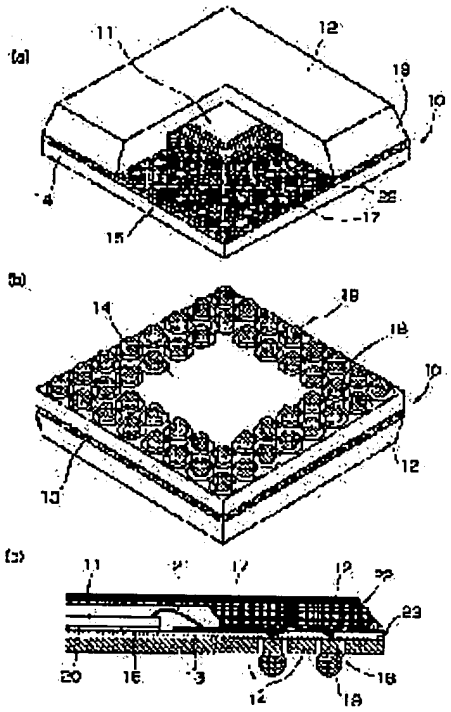
(54) SEMICONDUCTOR DEVICE, PACKAGE FOR SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To manufacture a semiconductor device excellent in humidity resistance, reliability and electric performance.
CONSTITUTION: A polyimide layer 13 and copper foil patterns 15, 17 are formed on plate type metal bases 14, 18, and a lamination structure body is constituted. The metal bases are constituted of a ground pattern 14 maintained at the earth potential and many land patterns 18 where solder balls 19 for mounting are formed. The copper foil patterns consist of an island pattern 15 where an LSI 11 is mounted and inner wiring 17 connected with the electrodes of the LSI chip 11. The metal base patterns 14, 18 are electrically connected with the internal wiring 17 via through-holes 22 formed by electroplating. A cap 12 covers the LSI 11 and the wiring pattern 17, and is bonded to the lamination structure body, thereby hermetically maintaining the internal space. A semiconductor device excellent in electric reliability and performance can be manufactured.



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CLAIMS

[Claim(s)]

[Claim 1] The package for semiconductor devices characterized by this grand pattern and a land pattern, and the aforementioned circuit pattern flowing through the aforementioned insulating layer through the through hole penetrated in a predetermined position including the grand pattern and two or more land patterns which are characterized by providing the following, and with which it was constituted as a laminated-structure object, and the aforementioned metal base pattern was insulated mutually electrically. The metal base pattern which consists of the metal plate which makes copper or aluminum a principal component, and has a predetermined pattern configuration. The insulating layer which consists of the organic system insulator formed on this metal base pattern at least. The thin film pattern which consists of the metallic foil which has the predetermined pattern configuration including a circuit pattern formed on this insulating layer.

[Claim 2] The package for semiconductor devices according to claim 1 in which a bump is formed on the aforementioned circuit pattern.

[Claim 3] The package for semiconductor devices according to claim 1 whose aforementioned thin film pattern has an island pattern for carrying a semiconductor chip.

[Claim 4] The package for semiconductor devices according to claim 1 constituted as a cavity to which the aforementioned thin film pattern and an insulating layer are removed, and the position in which a semiconductor chip is carried exposes the aforementioned metal base pattern.

[Claim 5] The claim 1 which some aforementioned grand patterns [at least] consist of as a ring pattern arranged in the shape of a frame at the periphery section of the aforementioned laminated-structure object, or the package for semiconductor devices given in any 1 of 4.

[Claim 6] The claim 1 from which the aforementioned metal base pattern consists of a ring pattern arranged in the shape of a frame at the periphery section of the aforementioned laminated-structure object, a central pattern which had the circumference surrounded by this ring pattern, and two or more aforementioned land patterns, and either [at least] the aforementioned ring pattern or a central pattern constitutes the aforementioned grand pattern, or the package for semiconductor devices given in any 1 of 4.

[Claim 7] The package for semiconductor devices according to claim 6 by which a chip is arranged between the aforementioned ring pattern and the aforementioned central pattern.

[Claim 8] The claim 1 further equipped with the insulating resin layer which coats the front face of the aforementioned metal base patterns other than the aforementioned land pattern, and the crevice portion of this metal base pattern, or the package for semiconductor devices given in any 1 of 7.

[Claim 9] The claim 1 through which is equipped with the combination of 1 more or more sets of another insulating layers, and a thin film pattern on the aforementioned thin film pattern, and the thin film pattern which counters mutually flows through the through hole formed in the predetermined position of the insulating layer which intervenes between [this] thin film patterns, or the package for semiconductor devices given in any 1 of 8.

[Claim 10] The package for semiconductor devices containing the ring closure pattern with which the aforementioned thin film pattern of the best layer is arranged in the shape of a frame at the periphery section of a laminated-structure object according to claim 9.

[Claim 11] The claim 1 in which the aforementioned thin film pattern contains the ring closure pattern arranged in the shape of a frame at the periphery section of the aforementioned laminated-structure object, or the package for semiconductor devices given in any 1 of 8.

[Claim 12] The claim 1 which the aforementioned thin film pattern and an insulating layer are removed in the shape of a frame in the periphery section of the aforementioned laminated-structure object, and a metal base pattern is exposed in the this removed periphery section, and constitutes the ring closure section, or the package for semiconductor devices given in any 1 of 8.

[Claim 13] The claim 1 in which the aforementioned through hole is formed of plating, or the package for semiconductor devices given in any 1 of 12.

[Claim 14] The package for semiconductor devices characterized by having joined the laminated-structure object of both this mutually through the middle insulating layer so that it might have a claim 1 or two laminated-structure objects given in any 1 of 9 and the aforementioned thin film pattern might face each other, and for the thin film pattern of the laminated-structure

object of both this having flowed through the through hole formed in the predetermined position in a middle insulating layer, and the metal base pattern of one laminated-structure object containing a flip chip bump.
[Claim 15] The semiconductor device characterized by being attached in the aforementioned laminated-structure object with the bonding which is equipped with the semiconductor chip carried in a claim 1 and a claim 3, or the package for semiconductor devices and this package given in any 1 of 13, and this semiconductor chip depends for any of an organic system resin, a metal mixing resin, or a low melting point metal being.
[Claim 16] The semiconductor device characterized by having the semiconductor chip carried in the package for semiconductor devices and this package according to claim 2, and carrying out flip chip bonding of this semiconductor chip through a resin or a low melting point metal on the aforementioned bump.
[Claim 17] The semiconductor device according to claim 15 or 16 further equipped with the cap of the metal which closes airtightly the thin film pattern side of the aforementioned laminated-structure object, or the product made of an organic resin.
[Claim 18] The claim 15 which each of the aforementioned land pattern equips with a solder ball, or a semiconductor device given in any 1 of 17.
[Claim 19] The claim 15 which equips the lower part of the aforementioned semiconductor chip with the thermolysis through hole which penetrates the aforementioned grand pattern at least and by which the thermolysis solder ball was formed in the position which adjoins the thermolysis through hole of this grand pattern, or a semiconductor device given in any 1 of 18.
[Claim 20] The manufacture method of the package for semiconductor devices which is the method of manufacturing the package for semiconductor devices according to claim 14, and is characterized by performing the aforementioned junction by either adhesives, thermocompression bonding or the adhesion using the chemical reaction.
[Claim 21] The 2nd opening is formed in the process which forms the thin film pattern characterized by providing the following, and the position adjusted in the 1st opening of the above of the aforementioned insulating layer. A deposit is formed in 2 openings. the [that exposes the aforementioned metal base in this 2nd opening / a process, the above 1st, and] -- The manufacture method of the package for semiconductor devices which carries out patterning of the process which makes it flow through the aforementioned metal base and the aforementioned thin film pattern, and the aforementioned metal base, and is characterized by including the process formed in two or more patterns insulated mutually. The insulating layer which consists of an organic system insulator on the metal base which consists of the metal plate which makes copper or aluminum a principal component. Patterning of the process and the aforementioned metallic foil layer which carry out the laminating of the metallic foil layer one by one, and form a laminated-structure object is carried out, and it is the 1st opening.

[Translation done.]